942 Register No.:

April 2018

Time – Three hours
(Maximum Marks: 75)

[N.B: (1) Q.No. 8 in PART – A and Q.No. 16 in PART – B are compulsory. Answer any FOUR questions from the remaining in each PART – A and PART – B

(2) Answer division (a) or division (b) of each question in PART – C.

(3) Each question carries 2 marks in PART – A, 3 marks in Part – B and 10 marks in PART – C.]

PART – A

1. Draw the structure of a control unit.
2. What are the various phases in instruction cycle?
3. Mention the types of 8 bit data transfer between two units.
4. Why we need refreshing in DRAM?
5. What is a flag register in a CPU?
6. What is page replacement technique?
7. Distinguish a user level thread from a kernel level thread.
8. Define vector interrupt.

PART – B

9. Explain the PUSH and POP operations in a memory stack.
10. Mention the transmitter function of an asynchronous communication interface.
11. Define hit ratio.
12. What are super scalar pipelines?
13. Explain about the various segment registers of 8086.
14. Distinguish thread from process.
15. List the pros and cons of NUMA.
16. What is IOP?

[Turn over.....

PART – C

17. (a) (i) Draw and explain 4 bit arithmetic circuit.
(ii) Explain execute cycle in detail.

(Or)

(b) Explain the zero address, one, two and three address instructions with example.

18. (a) (i) Explain daisy chain priority.
(ii) Explain source initiated strobe control with a diagram.

(Or)

(b) Explain DMA transfer.

19. (a) (i) Write about different types of memory.
(ii) Explain the page replacement techniques in detail.

(Or)

(b) Draw a memory table for main memory capacity of 8kB and secondary memory capacity of 16kB for a paged system.

20. (a) (i) Mention the different applications of microprocessor.
(ii) Explain the various blocks in execution unit of 8086 microprocessor.

(Or)

(b) Draw and explain the various stages of arithmetic pipeline in detail.

21. (a) (i) Distinguish a SMP from a cluster.
(ii) Write about different approaches to explicit multithreading.

(Or)

(b) Explain the organization and features of core 2 duo processor.
